An Energy Harvesting Chip designed to Extract Maximum Power from a TEG

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Abstract— In this paper, we present measurement results from a prototype chip (fabricated in 130 nm CMOS technology), designed to extract maximum power from a Thermoelectric Generator (TEG). From analytical expression, we prove that the maximum extracted power is around 75% of the available power in a TEG, without using a closed loop maximum peak power tracking to regulate the input voltage. In our measurements, the TEG is modeled by a voltage source (50mV-200mV) with a series resistance of 5 Ohms. The prototype is fully electric, starts from 50 mV and can extract 60% (at 50 mV) to 65% (at 200 mV) of the available power. Hence the measurement result closely agrees with the analytical expression.

Keywords- Available power; Extracted power; Energy harvesting; Low voltage; Thermo-electric generator

I.   INTRODUCTION

DC-DC converters have been attractive devices for elevating low voltage to high voltage in low power applications [1]. Their use has been reported in wearable electronics, powering sensor nodes, charging batteries in solar cell, etc. The most popular techniques for DC-DC conversion are the use of the switched capacitor method, or inductively charging a capacitor. The latter is more efficient and has also been widely reported in the literature. A common type of sensor used to convert thermal voltage to electrical voltage is a Thermoelectric Generator (i.e., TEG) [2]. Work have been reported to convert the output of a TEG, which is typically around 50 mV to around 1 V, so that it can power any load, which can be an electronic circuit or a rechargeable battery [2]. The DC-DC converter can be self-starting, or start by external means. The startup voltage, startup time and efficiency of the converter circuit are areas of improvement.

This article discusses two topics: 1. The availability of power and maximum power that can be extracted from a TEG using an ideal converter, 2. The Measurement results obtained from the converter circuit implemented in 130 nm CMOS technology, able to extract almost the maximum power (excluding losses and the power consumption of the circuit) from the TEG. The implemented circuit can extract power from both the half cycles of the clock using Zero Current Switching (i.e., ZCS) technique [3], [4]. The measurement results from one chip shows improvement in startup time and efficiency [5]. The layout of this paper is

as follows: Section II, derive the analytical result about power that can be extracted from available power using an ideal converter. In Section III, we present the circuit schematic and discuss some important blocks. Finally, Section IV presents the measurement results, and in Section V we draw some conclusions.

II.   POWER THAT CAN BE EXTRACTED FROM THE AVAILABLE POWER

Fig. 1 shows the schematic of the circuit configuration used for this derivation. The circuit does not use any input capacitance (C_{IN}) at the V_{IN} node. In Fig. 1, the available power is given by,

$$P_{AV} = \frac{V_{TEG}^2}{4 \cdot R_{TEG}} . \qquad (1)$$
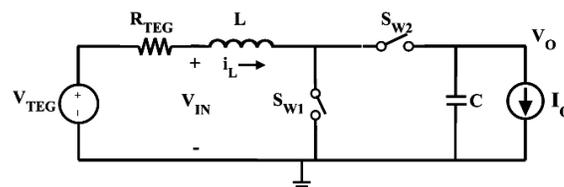
Figure 1.   An ideal switch S_{W1} is used to charge the inductor and switch S_{W2} is used to discharge the inductor (L) in capacitor (C). I_O is the load current. The TEG is modelled by voltage source V_{TEG} and internal resistance R_{TEG}.

Fig. 2 shows the behaviour of the current in L over a complete clock cycle T_{SW} in Discontinuous Conduction Mode (i.e., DCM) [6].
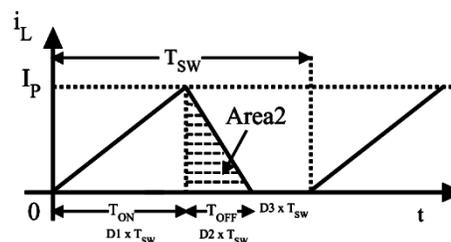
Figure 2.   D1, D2, and D3 are the duty cycles respectively. The "L" is charged during T_{ON} by closing S_{W1} and opening S_{W2} and then discharged during T_{OFF} by opening S_{W1} and closing S_{W2}. After T_{OFF}, the convertor is in the idle state (D3 × T_{SW}). Area 2 = ½ × T_{OFF} × I_P, where I_P is the inductor peak current.

The Area2 in Fig. 2 shows the energy available to the load, and this can be expressed as,

$$\text{Area2} = I_O \cdot T_{SW} = \frac{I_P \cdot D2 \cdot T_{SW}}{2} \ . \tag{2}$$

Solving (2), the average value of load current is,

$$I_O = \frac{D2 \cdot I_P}{2} \ . \tag{3}$$

The power delivered to the load (lossless converter) is,

$$P_O = \frac{1}{T_{SW}} \int_0^{T_{SW}} p(t) \ dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} \left(V_{TEG} - R_{TEG} \cdot i_{TEG} \right) \cdot i_{TEG} \ dt \ . \tag{4}$$

$$
\begin{aligned}
T_{SW} \times P_O = & \int_0^{T_{ON}} \left(V_{TEG} - R_{TEG} \frac{I_P \cdot t}{T_{ON}} \right) \frac{I_P \cdot t}{T_{ON}} \ dt \\
& + \int_{T_{ON}}^{T_{ON}+T_{OFF}} \left[V_{TEG} - R_{TEG} \frac{I_P \cdot (T_{ON}+T_{OFF}-t)}{T_{OFF}} \right] \frac{I_P \cdot (T_{ON}+T_{OFF}-t)}{T_{OFF}} \ dt
\end{aligned} \tag{5}
$$

On solving and rearranging (5), we will get

$$T_{SW} \times P_O = \left| \frac{V_{TEG}}{2} - \frac{R_{TEG} I_P}{3} \right| (T_{ON}+T_{OFF}) I_P \ . \tag{6}$$

For the power to be max,

$$\frac{dP_O}{dI_P} = 0 \rightarrow \frac{V_{TEG}}{2} - \frac{2 \cdot R_{TEG} I_{Pmax}}{3} = 0 \Rightarrow I_{Pmax} = \frac{3}{4} \frac{V_{TEG}}{R_{TEG}} \ . \tag{7}$$

From (3), the maximum output current,

$$I_{Omax} = \frac{D2 \cdot I_{Pmax}}{2} = D2 \frac{3}{8} \frac{V_{TEG}}{R_{TEG}} \ . \tag{8}$$

From (6), the maximum output power,

$$P_{Omax} = (D1 + D2) \cdot \frac{3}{4} \frac{V_{TEG}^2}{4 \cdot R_{TEG}} \ . \tag{9}$$

Defining the efficiency as the ratio between the output power and the available power, so we can write

$$\eta = \frac{P_{Omax}}{P_{AV}} = (D1 + D2) \frac{3}{4} \times 100\% \ . \tag{10}$$

In case of symmetrical clock used for switching in a high gain situation, $D1 + D2 \approx D1$ ($\equiv 0.5$), therefore (10) can be numerically expressed as

$$\eta = \frac{3}{8} \times 100 \ \% . \tag{11}$$

Therefore, it can be concluded that an ideal converter can extract 37.5% of the available power in one half cycle. If both half cycles are used, then the maximum output power that can be possible to obtain, is 75% of the input available power.

A. Selecting the value of L to extract available power

In Fig. 1, let us consider that a current i_L flow when switch S_{W1} is closed, and inductor get charged to peak value I_P for the time T_{ON}. The peak value of this current will be discharged to load when switch S_{W1} opens and switch S_{W2} closes [6]. Therefore the output power (P_O) to the load is $P_O = I_O \times V_O$, can be expressed as

$$P_O \approx \left(\frac{V_{TEG}}{R_{EQ}} \right)^2 \left(1 - \exp\left(-\frac{T_{ON} R_{EQ}}{L} \right) \right)^2 \frac{L}{2 \cdot T_{SW}} \ . \tag{12}$$

In (12), $R_{EQ} = R_{SW} + R_{IND} + R_{TEG}$, R_{IND} is the internal resistance of the inductor, and R_{SW} is the resistance of the switch. Eq. (12) is the P_O obtained from one half of the cycle (T_{ON}), and it can be multiplied by 2, when the inductor is energized for both halves of a cycle. In (12), to know the value of the inductor that can extract maximum power P_O, we can sweep L (x- axis) and note peak value of P_{Omax} (y-axis). And for the corresponding peak value, we get the value of L [5].

III. PROPOSED CIRCUIT TO EXTRACT MAXIMUM POWER

The overall architecture of the circuit is shown in Fig. 3. It is composed by a Main Stage, containing the MOS transistors implementing the low Vt switches NM1, 2 and PM1, 2, 3, plus the off-chip inductance and a divider to obtain the voltage references, and an Auxiliary stage, whose duty cycle is to generate the proper biasing and the control signals for the switches. The auxiliary convertor is driven by a Low Voltage Starter (i.e., LVS is shown in Fig. 4), which is a two stage Enhanced Swing Ring Oscillator (i.e., ESRO) [7], which starts up at around 30 mV. The LVS also has a 12 stage Dickson Charge Pump (i.e., DCP) [8], that converts the AC swing into a DC voltage used to start the first Current Starved Ring Oscillator (i.e., CSRO-1). At the 500 mV output from the DCP, the CSRO-1 oscillates with a time period of 10 µs. And drives an auxiliary boost convertor stage, which consist of an NMOS switch (NM0), a low V_t on-chip diode and an external inductor L_{AUX}. Through an external inductor the auxiliary convertor boosts the voltage at V_{DDi} node to 600 mV, the V_{DDi} node has an on-chip capacitor of 1nF. With this capacitor value the ripple at V_{DDi} is around 20 mV (p). The peripherals at V_{DDi} node consume a current of 1.5 µA at 600 mV and 4 µA at 1 V.
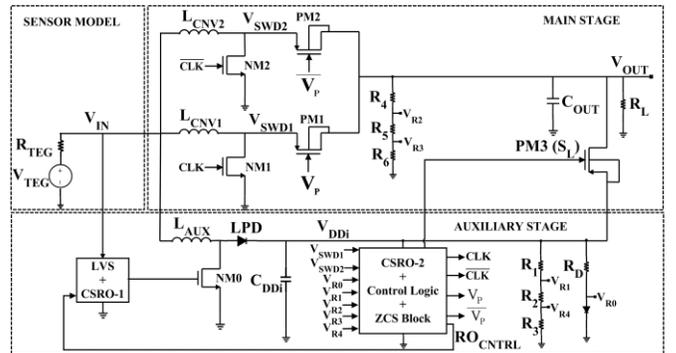
Figure 3.   Simplified block diagram of the circuit. NM mean NMOS switch and PM mean PMOS switch. (W/L); NM1, 2: 480 × 4 µm /0.12 µm, PM1, 2: 120 × 4 µm /0.12 µm, NM0: 48× 4 µm /0.48 µm, PM3: 3×4 µm/0.12 µm.
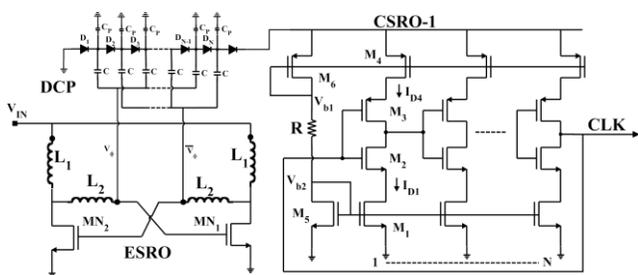
Figure 4. LVS block showing ESRO + DCP + CSRO-1. $MN_{1,2}$ are Zero Vt transistors. C and C_P are the coupling and parasitic capacitance respectively. R is around 8 MΩ and is present on the chip. The CLK is passed through the chain of three inverters (minimum W and L), to drive NM0 in Fig. 3.
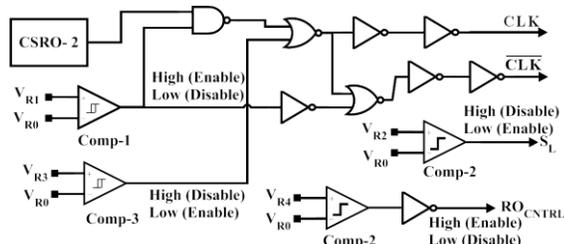
Figure 5. Control logic to regulate the V_{OUT} in the circuit of Fig. 3. It is also used to drive switches in the main and auxiliary stage in Fig. 3.
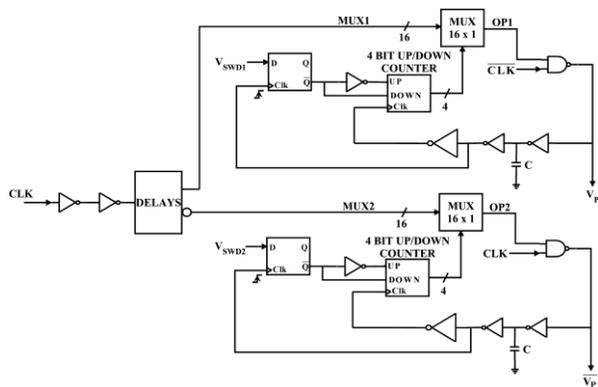
Figure 6. Zero Current Switching scheme to control the switches PM1, 2.

Once V_{DDi} reaches 600 mV, the peripheral circuits shown in Fig. 5 and Fig. 6, start to work. Another CSRO-2 (similar to CSRO-1 in Fig. 4, but with different transistor aspect ratio), provides a clock of 40 µs at 600 mV for the $L_{CNV1, 2}$, and using a control logic, complementary clocks were generated to drive the switches NM-1, 2. A Zero Current Switching (ZCS) network as shown in Fig. 6, generate pulses to close and open the switches PM-1, 2. In Fig. 6, the delay block generates 16 delays in the range of 0.5 µs - 2.5 µs, to cover the 50 mV - 200 mV of the TEG voltage, maintaining the 10 mV voltage resolution. The sequential search algorithm was used to choose one of the delay [4], according to the rising or falling edge of the $V_{SWD1, 2}$ polarity, with respect to the pulse V_P/ $V_{P\,bar}$. A value of C = 0.21 pF was chosen in Fig. 6, to introduce the loop delay between $V_{SWD1, 2}$ and V_P/ $V_{P\,bar,}$ according to the [9, Fig. 3].
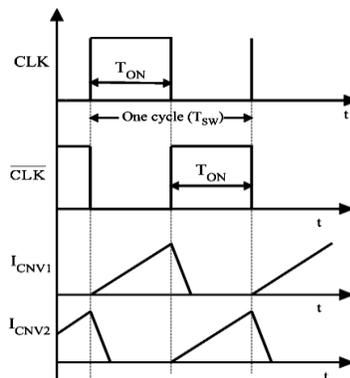
Figure 7. Clock scheme to control the switches, NM1, PM1, NM2 and PM2. The figure also shows the charging and discharging of currents through the inductors L_{CNV1} and L_{CNV2}. For simplicity, T_{OFF} for switches PM1 and PM2 are not shown in the figure [5].

The switch S_L is closed to boost the V_{OUT} from 600 mV to 1 V. In our design the inductors are energized separately for two cycles of the clock pulses as shown in Fig. 7. Using this technique we can extract more than 50% of the maximum available power from the TEG. Reference voltages are generated at V_{DDi} and V_{OUT} nodes and to regulate the power, we have used comparators based control logic shown in Fig. 5. The output voltage is regulated close to 1 V.

IV. MEASUREMENT RESULTS

In this section measurement results of the prototype circuit are reported. To measure the transient response of the chip, we have used a source measure unit and a 5 Ω resistance in series. The setup was used to emulate the model from a Tellurex TEG, which has a sensitivity of 25 mV/K [3]. To the output of the chip, a potentiometer was connected as a load, and the measurements were recorded. Fig. 8 shows the picture of the die realizing our proposed circuit.
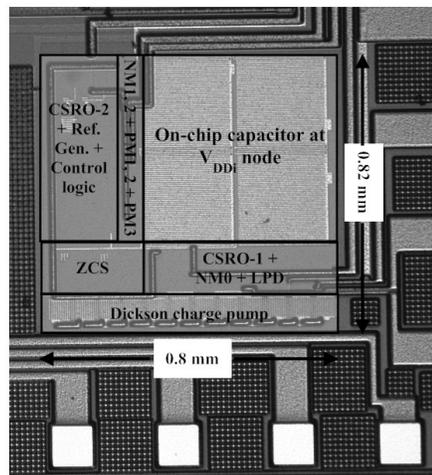
Figure 8. Photo of the die implementing the circuit shown in Fig. 3.

The values of external components used in our work are: C_{OUT} = 26 nF, R_{OUT} (a potentiometer) = 0 – 50 KΩ, $L_{CNV1, 2}$ = 100 µH, L_{AUX} = 330 µH, ESRO: L_1 = 0.47 mH and L_2 = 2.2 mH. The definition of efficiency (i.e., η) in this work is,

$$\eta = \frac{P_{OUT}|_{V_{OUT} = 1V}}{P_{AV}} \times 100\% . \tag{13}$$

In (13), V_{OUT} is the voltage across the load, which in our work is nearly equal to one volt. However, this voltage will depend on the reference generator susceptibility to process variation. In the coming figures, we will present some transient response at the output of the chip, by varying the input voltage.

Fig. 9 – 10, show the response of the chip for two different values of the input voltage, Ch2 (trace in blue) corresponds to V_{OUT} and Ch1 (trace in light blue) corresponds to V_{DDi}. Figures indicate that the V_{DDi} and V_{OUT} closes at 600 mV and the output is boosted to 1 V. This clearly demonstrates the working of the prototype chip. The output is regulated, therefore when the input is varied to high voltage and load is kept constant, the voltage is around 1 V only. By using the circuit configuration shown in Fig. 3, we got a transient settling time of 4 ms at 50 mV. In [3] and [4], transient settling time of more than 15 ms is reported, thus we have improved circuit startup time.
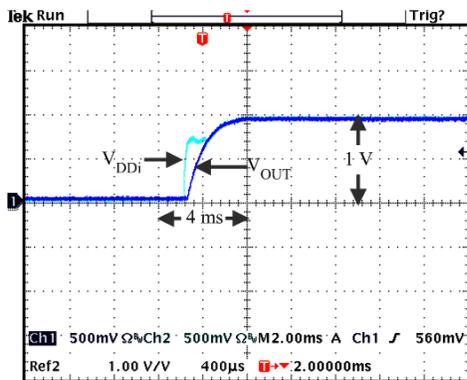
Figure 9.   Transient response when V_{TEG} = 50 mV.
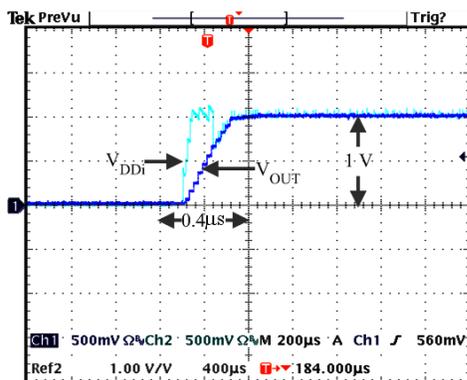
Figure 10. Transient response when V_{TEG} = 150 mV.
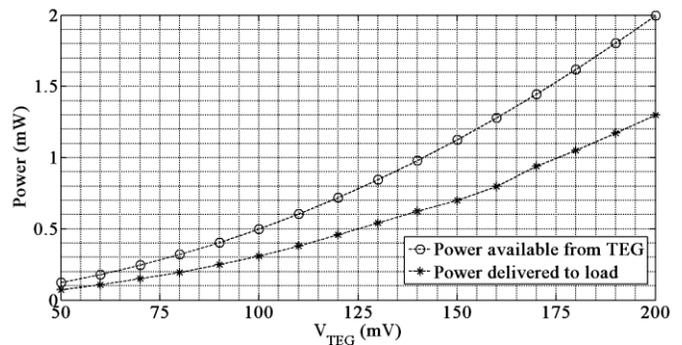
Figure 11. The plot shows the available power and delivered load power for a TEG. The voltage range covers the TEG temperature range from 2 ^{0}K to 8 ^{0}K.

Fig. 11 shows the plot of power for the entire range of TEG voltage. The efficiency varies from 60% to 65% at 50 mV and 200 mV respectively. This closely matches with our derivation on the extraction of maximum power from available power. The dynamic and static power loss (at 1 V), due to switches NM1, 2 are 57.12 nW and 2.52 µW, which is acceptable. Around 4 µW is consumed by the peripherals, and the rest of the power is lost because of transient during switching.

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